IN THE CLAIMS

1. (Previously Presented) A microprocessor comprising:

at least one throttling mechanism; and

a thermal control subsystem to estimate an amount of power used by said microprocessor and to control said at least one throttling mechanism based on said estimated power usage, wherein the thermal control subsystem is in communication with at least one counter and the thermal control subsystem estimates the amount of power used by the microprocessor based on information provided by the at least one counter.

2. (Original) The microprocessor of claim 1, wherein the amount of power used by the microprocessor is estimated based on the number of occurrences of at least one activity performed in said microprocessor.

3. (Original) The microprocessor of claim 1, wherein thermal control subsystem includes a power usage monitoring unit which determines the number of occurrences of at least one activity performed by the microprocessor within a sampling time period and computes the estimated power usage based on (1) the count value associated with said at least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor

4. (Original) The microprocessor of claim 3, wherein the power usage monitoring unit estimates the amount of the power used by the microprocessor by averaging the current estimated power usage value with a defined number of most recently estimated power usage values obtained during previous sampling time periods.

5. (Original) The microprocessor of claim 1, wherein the thermal control subsystem further comprises a throttling control unit which compares said estimated amount of power used by the microprocessor against a threshold and activates the throttling mechanism if the estimated power used by the microprocessor is greater than said threshold or deactivates the throttling mechanism if the estimated power used by the microprocessor is less than said threshold.

6. (Original) The microprocessor of claim 1, wherein the throttling mechanism is activated in a deterministic manner by the thermal control subsystem.

7. (Original) The microprocessor of claim 2, wherein said at least one activity monitored by the thermal control subsystem comprises at least one of the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding.

8. (Previously Presented) A method comprising:

receiving information provided by at least one counter;

estimating an amount of power used by a microprocessor based on the information provided by the at least one counter; and

controlling at least one throttling mechanism incorporated in the microprocessor based on said estimated power usage.

9. (Original) The method of claim 8, wherein the amount of power used by the microprocessor is estimated based on the number of occurrences of at least one activity performed in the microprocessor.

10. (Original) The method of claim 8, wherein the estimating the amount of power used by the microprocessor further comprises:

counting the number of occurrences of at least one activity performed by the microprocessor within a sampling time period; and

adjusting the number of occurrences of said at least one activity according to current operating frequency and voltage level of the microprocessor.

11. (Original) The method of claim 10, wherein the estimating the amount of the power used by the microprocessor further comprises averaging the current estimated power usage value with a defined number of most recently estimated power usage values obtained during previous sampling time periods.

12. (Original) The method of claim 8, further comprising:

comparing said estimated amount of power used by the microprocessor against a threshold;

activating said at least one throttling mechanism if said estimated power used by the microprocessor is greater than said threshold; and

deactivating said at least one throttling mechanism if said estimated power used by the microprocessor is less than said threshold.

13. (Original) The method of claim 8, wherein the throttling mechanism is activated in a deterministic manner.

14. (Original) The method of claim 10, wherein said at least one activity monitored is selected from the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding.

15. (Previously Presented) A thermal control system comprising:

a power usage estimator coupled to at least one counter, the power usage estimator to estimate an amount of power used by a microprocessor based on information provided by the at least one counter; and

a throttling control unit to control at least one throttling mechanism incorporated in the microprocessor based on the estimated amount of power used by the microprocessor.

16. (Original) The thermal control system of claim 15, wherein said power usage estimator estimates the amount of power used by the microprocessor based on (1) the number of occurrences of at least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor.

17. (Original) The thermal control system of claim 15, further comprising a filter to adjust the estimated amount of power usage by applying recently estimated power usage values obtained during previous sampling time periods with the current estimated power usage value.

18. (Original) The thermal control system of claim 15, wherein said throttling control unit compares said estimated amount of power used by the microprocessor against a threshold and activates the throttling mechanism if the estimated power used by the microprocessor is greater than said threshold or deactivates the throttling mechanism if the estimated power used by the microprocessor is less than said threshold.

19. (Previously Presented) A machine-readable medium that provides instructions, which when executed by a microprocessor cause said microprocessor to perform operations comprising:

receiving information provided by at least one counter;

estimating an amount of power used by a microprocessor based on the information provided by the at least one counter; and

controlling at least one throttling mechanism incorporated in the microprocessor based on said estimated power usage.

20. (Original) The machine-readable medium of claim 19, wherein the amount of power used by the microprocessor is estimated based on the number of occurrences of at least one activity performed in the microprocessor.

21. (Original) The machine-readable medium of claim 19, wherein the operation of estimating the amount of power used by the microprocessor further comprises reading count data representing the number of occurrences of at least one activity performed by the microprocessor within a sampling time period and adjusting the number of occurrences of said at least one activity according to current operating frequency and voltage level of the microprocessor.

22. (Original) The machine-readable medium of claim 21, wherein the operation of estimating the amount of the power used by the microprocessor further comprises averaging the current estimated power usage value with a defined number of most recently estimated power usage values obtained during previous sampling time periods.

23. (Original) The machine-readable medium of claim 19, wherein the operations further comprises:

comparing said estimated amount of power used by the microprocessor against a threshold;

activating said at least one throttling mechanism if said estimated power used by the microprocessor is greater than said threshold; and

deactivating said at least one throttling mechanism if said estimated power used by the microprocessor is less than said threshold.

24. (Original) The machine-readable medium of claim 19, wherein the throttling mechanism is activated in a deterministic manner.

25. (Original) The machine-readable medium of claim 21, wherein said at least one activity monitored is selected from the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding.

26. (Previously Presented) The microprocessor of claim 1, wherein the at least one counter is implemented as a register in a hardware component.

27. (Previously Presented) The microprocessor of claim 1, wherein the at least one counter is implemented as a variable in software code.